R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments and new claim may be found in the specification, for example, on page 6, lines 12-17, FIGS. 2 and 3 and claims 14 and 20, as originally filed. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-20 under 35 U.S.C. §102 as being anticipated by Ginetti et al. '658 (hereafter Ginetti) is respectfully traversed and should be withdrawn.

Ginetti concerns a method and a system for specifying and automatically analyzing multiple clock timing constraints in a VLSI circuit (Title). In contrast, the present invention provides a method for generating a plurality of timing constraints for a circuit design. The method generally comprises the steps of (A) identifying a plurality of clock signals by analyzing the circuit design, (B) determining a plurality of relationships among the clock signals and (C) generating the timing constraints for the circuit design in response to the clock signals and the relationships.

Claim 1 provides (in part) a step for (A) identifying a plurality of clock signals by analyzing a circuit design. Despite the assertion on page 2 of the Office Action, FIG. 1 of Ginetti and the text in column 2, lines 23-61 of Ginetti appear to be silent regarding a method step for (i) analyzing a circuit design to (ii) identify multiple clock signals. In particular, the cite by the Office Action to a figure in Ginetti having two clock signals does not establish a step for identifying by analyzing. Therefore, the Office Action has failed to establish that Ginetti discloses or suggests a step for identifying a plurality of clock signals by analyzing a circuit design as presently claimed. Claims 14 and 20 provide language similar to claim 1, step (A) The Examiner is respectfully requested to either (i) provide clear and concise evidence where Ginetti expressly or inherently discloses the claimed method step for identifying or (ii) withdraw the rejection.

Claim 1 further provides a step for (B) determining a plurality of relationships among a plurality of clock signals. Despite the assertion on page 2 of the Office Action, FIGS. 1-5 and the text in column 2, lines 23-61 and column 3 line 16-column 4 line 64 of Ginetti appear to be silent regarding a method step for determining relationships among clock signals. Therefore, the Office Action has failed to establish that Ginetti discloses or suggests a step for determining a plurality of relationships among a plurality of clock signals as presently claimed. Claim 20

provides language similar to claim 1, step (B). The Examiner is respectfully requested to either (i) provide clear and concise evidence where Ginetti expressly or inherently discloses the claimed determining step or (ii) withdraw the rejection.

Claim 1 further provides a step for (C) generating a plurality of timing constraints for a circuit design in response to a plurality of clock signals and a plurality of relationships among the clock signals. Despite the assertion on page 2 of the Office Action, FIGS. 1-5 and the text in column 4 line 65-column 7, line 8, the "summary" and column 9 line 60-column 10 line 44 of Ginetti appear to be silent regarding a method step for generating timing constraints based on clock signals and relationships among the clock signals. Therefore, the Office Action has failed to establish that Ginetti discloses or suggests a step for generating a plurality of timing constraints for a circuit design in response to a plurality of clock signals and a plurality of relationships among the clock signals as presently claimed. Claim 20 provides language similar to claim 1, step (C). The Examiner is respectfully requested to either (i) provide clear and concise evidence where Ginetti expressly or inherently discloses the claimed generation step or (ii) withdraw the rejection. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 14 further provides a step for (B) querying a user for a plurality of parameters for a plurality of clock signals. In contrast, (i) Ginetti appears to be silent and (ii) the Office Action makes no arguments regarding a method or process querying a user for clock signal parameters. Therefore, Ginetti does not appear to disclose or suggest a step for querying a user for a plurality of parameters for a plurality of clock signals as presently claimed.

Claim 14 further provides a step for (C) generating a plurality of timing constraints in response to a plurality of clock signals and a plurality of parameters for the clock signals queried from a user. In contrast, (i) Ginetti appears to be silent and (ii) the Office Action makes no arguments regarding generation of timing constraints responsive to clock signals and user provided parameters for the clock signals. Therefore, Ginetti does not appear to disclose or suggest a step for generating a plurality of timing constraints in response to a plurality of clock signals and a plurality of parameters for the clock signals queried from a user as presently claimed. As such, claim 14 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 20 further provides a medium recording a computer program including the steps of claim 1. In contrast, (i) Ginetti appears to be silent and (ii) the Office Action makes no arguments regarding a medium disclosed by Ginetti recording a computer

program including steps for identifying clock signals, querying a user for parameters and generating timing constraints. Therefore, Ginetti does not appear to disclose or suggest a medium recording a computer program as presently claimed. As such, claim 20 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 2 provides a plurality of clock signals comprising a test clock signal. In contrast, Ginetti appears to be silent regarding test clock signals. Therefore, Ginetti does not appear to disclose or suggest a plurality of clock signals comprising a test clock signal as presently claimed. The Examiner is respectfully requested to either (i) clearly identify by name any clock signal disclosed by Ginetti that is allegedly similar to the claimed test clock signal or (ii) withdraw the rejection. Claims 6 and 12 also provide test clock signals. As such, claims 2, 6 and 12 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 3 provides a step for eliminating a respective timing constraint of a plurality of timing constraints for each signal connected to an internal pin for a circuit design that defines a non-clock signal. In contrast, Ginetti appears to be silent regarding a method step for removing timing contrasts. Therefore, Ginetti does not appear to disclose or suggest a step for eliminating a respective timing constraint of a plurality of

timing constraints for each signal connected to an internal pin for a circuit design that defines a non-clock signal as presently claimed. The Examiner is respectfully requested to either (i) explain how the cited figures and text of Ginetti disclose eliminating timing constraints as claimed or (ii) withdraw the rejection. Claims 4 and 7 provides a similar eliminating step as claim 3. As such, claims 3, 4 and 7 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 8 provides a step for generating an asynchronous relationship of a plurality of relationships among a plurality of clock signals between at least two of the clock signals operating asynchronously to each other. In contrast, Ginetti appears to be silent regarding asynchronous clock signals. Therefore, Ginetti does nor appear to disclose or suggest a step for generating an asynchronous relationship of a plurality of relationships among a plurality of clock signals between at least two of the clock signals operating asynchronously to each other as presently claimed. The Examiner is respectfully requested to either (i) provide clear and concise evidence where Ginetti expressly or inherently discloses an asynchronous relationship among clock signals as claimed or (ii) withdraw the rejection.

Claim 9 provides a step for generating a fastest clock relationship of a plurality of relationships among a plurality of clock signals between at least two clock signals operating a

different speeds between two clock boundaries in a circuit design. In contrast, Ginetti appears to be silent regarding two clock boundaries of a circuit design. Therefore, Ginetti does not appear to disclose or suggest a step for generating a fastest clock relationship of a plurality of relationships among a plurality of clock signals between at least two clock signals operating a different speeds between two clock boundaries in a circuit design as presently claimed. The Examiner is respectfully requested to either (i) provide clear and concise evidence where Ginetti expressly or inherently discloses a relationship between two clocks operating at different speeds between two clock boundaries as claimed or (ii) withdraw the rejection.

Claim 10 provides a step for generating a multiplexed clock relationship of a plurality of relationships for a plurality of clock signals between at least two clock signals routable through a multiplexer in a circuit design. In contrast, Ginetti does not appear to disclose clock signals routable through multiplexers. Therefore, Ginetti does not appear to disclose or suggest a step for generating a multiplexed clock relationship of a plurality of relationships for a plurality of clock signals between at least two clock signals routable through a multiplexer in a circuit design as presently claimed. The Examiner is respectfully requested to either (i) provide clear and concise evidence where Ginetti expressly or inherently discloses routing

clock signals through a multiplexer as claimed or (ii) withdraw the rejection.

Claim 11 provides a step for generating a derivative clock relationship of a plurality of relationships among a plurality of clock signals between a first clock signal that is derived from a second clock signal. In contrast, Ginetti appears to be silent regarding a method step for deriving one clock signal from another clock signal. Therefore, Ginetti does not appear to disclose or suggest a step for generating a derivative clock relationship of a plurality of relationships among a plurality of clock signals between a first clock signal that is derived from a second clock signal as presently claimed. The Examiner is respectfully requested to either (i) provide clear and concise evidence where Ginetti expressly or inherently discloses a method step for generating a derivative clock signal relationship as claimed or (ii) withdraw the rejection.

Claim 13 provides a step for writing a plurality of timing constraints among a plurality of files. Despite the assertion on page 4 of the Office Action, Ginetti appears to be silent regarding multiple files storing timing constraints. In particular, Ginetti only appears to mention a single path-based constraint file 122 (see Ginetti column 10, lines 7-8). Therefore, Ginetti does not appear to disclose or suggest a step for writing a plurality of timing constraints among a plurality of files as

presently claimed. The Examiner is respectfully requested to either (i) clearly identify two or more files disclosed by Ginetti that allegedly store timing constraints as claimed or (ii) withdraw the rejection.

Claim 15 provides steps for (i) determining a plurality of relationships among a plurality of clock signals and (ii) generating a plurality of timing constraints in response to the clock signals, a plurality of parameters for the clock signals and the relationships among the clock signals. In contrast, Ginetti appears to be silent regarding steps for determining relationships among clock signals and generating timing constraints in response to the relationships. Therefore, Ginetti does not appear to disclose or suggest steps for (i) determining a plurality of relationships among a plurality of clock signals and (ii) generating a plurality of timing constraints in response to the clock signals, a plurality of parameters for the clock signals and the relationships among the clock signals as presently claimed. The Examiner is respectfully requested to either (i) provide clear and concise evidence where Ginetti expressly or inherently discloses steps for both determining relationships among clock signals as claimed and generating timing constraints in response to the relationships as claimed or (ii) withdraw the rejection.

Claim 16 provides a step for querying a user for a frequency parameter for each of a plurality of clock signals. In

contrast, Ginetti appears to be silent regarding querying a user for information. Therefore, Ginetti does not appear to disclose or suggest a step for querying a user for a frequency parameter for each of a plurality of clock signals as presently claimed. The Examiner is respectfully requested to either (i) provide clear and concise evidence where Ginetti expressly or inherently discloses querying a user for clock signal information as claimed or (ii) withdraw the rejection. Claim 17 provides querying language similar to claim 16. As such, claims 16 and 17 are fully patentable over the cited reference and the rejection should be withdrawn.

COMPLETENESS OF THE OFFICE ACTION

Aside from a notice of allowance, Applicants' representative respectfully requests any further action on the merits be presented as a **non-final** action. 37 CFR §1.104(b) states:

> (b) *Completeness of examiner's action.* The examiner's **action will be complete as to all matters**, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters of form need not be raised by the examiner until a claim is found allowable. (Emphasis added)

No arguments were presented directed to (i) two of the three claimed steps of independent claim 14 and (ii) the structure of

claim 20. Since no previous rejection were made to claims 14 and 20 the Action mailed April 7, 2004 was not complete.

The Examiner is respectfully requested to refrain from omnibus rejections that simply list all of the claimed elements and then assert that the claimed elements are disclosed somewhere among several figures and/or large sections of text (see MPEP 707.07(d)). Furthermore, MPEP §706.07 states:

> In making the final rejection, all outstanding ground of rejection of record should be carefully reviewed, and any such grounds relied on in the final rejection should be reiterated. They **must also be clearly developed to such an extent that applicant may readily judge the advisability of an appeal** unless a single previous Office action contains a complete statement supporting the rejection. (Emphasis added)

However, omnibus rejections generally are insufficiently clear to permit Applicants' representative to judge the advisability of an **appeal after the next Office Action**.

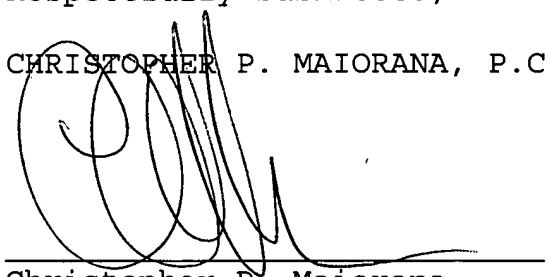
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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